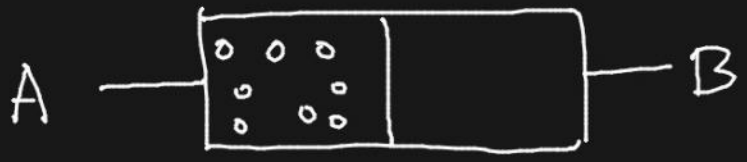
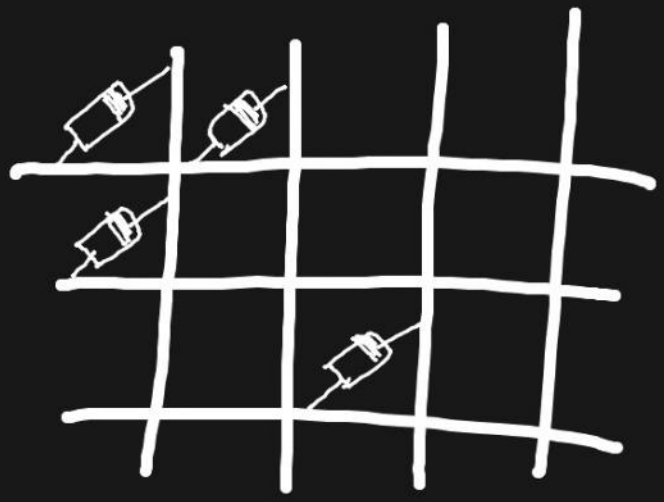


$V_{AB} > 0 \Rightarrow$ decrease in resistance

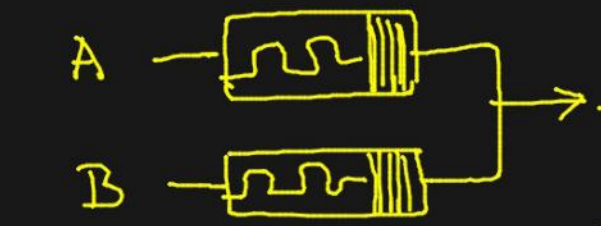
$V_{AB} < 0 \Rightarrow$ increase in resistance



Doped-Undoped Region

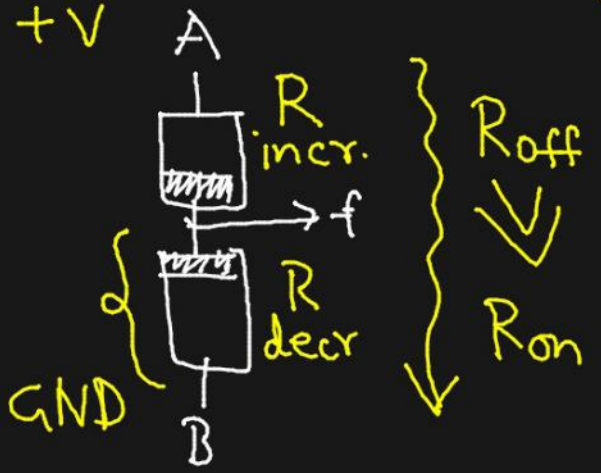
Logic Design :

(a) Memristor Ratioed Logic (MRL)



A	B	f
0	0	0
0	1	0
1	0	0
1	1	1

AND

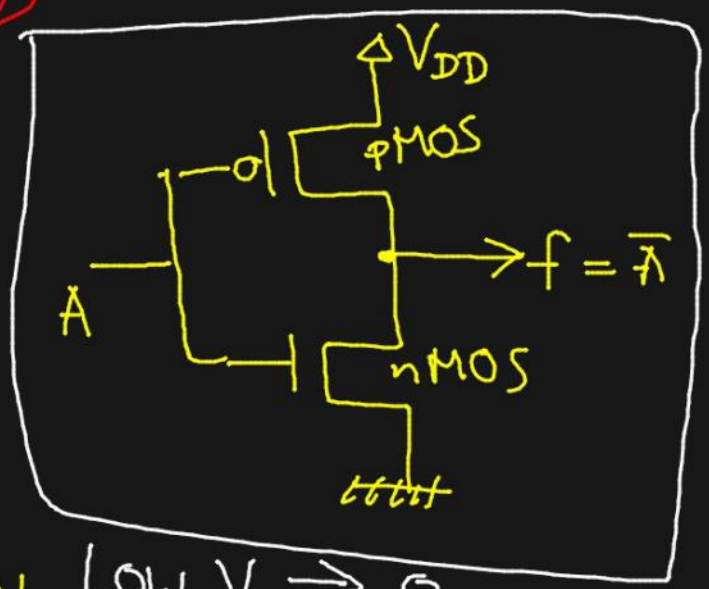


$$i = \frac{V}{R_{off} + R_{on}}$$

$$f = i \cdot R_{on} \simeq \frac{R_{on}}{R_{on} + R_{off}} \cdot V$$

$$\approx 0V$$

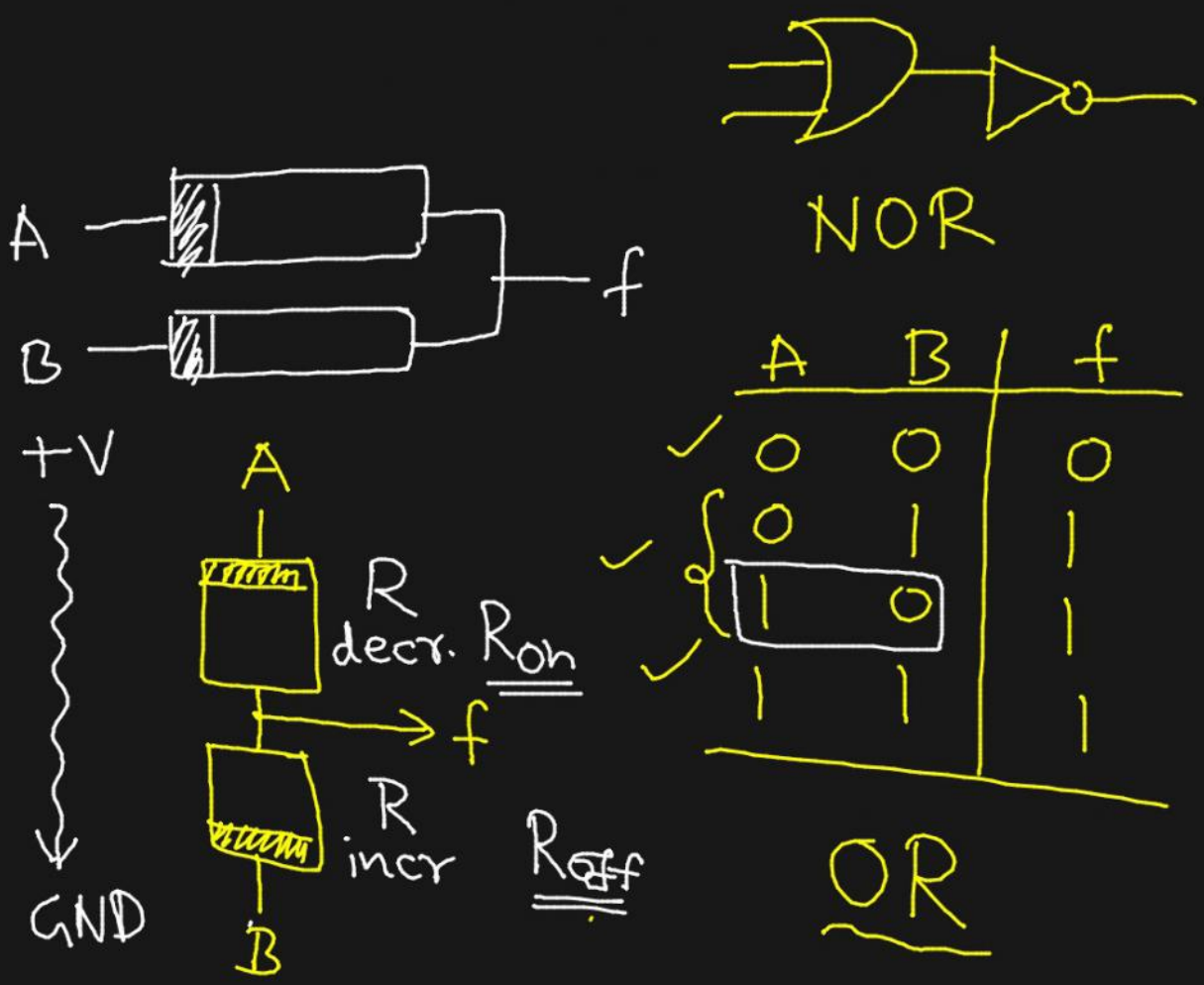
CMOS inverter



Low V ⇒ 0

High V ⇒ 1

MRL-AND-with-Inverter



$$R_{off} \gg R_{on}$$

$$f = \frac{R_{off}}{R_{off} + R_{on}} \cdot V$$

$$= \frac{1}{1 + R_{on}/R_{off}} \cdot V$$

$$\approx V$$

MRL-OR

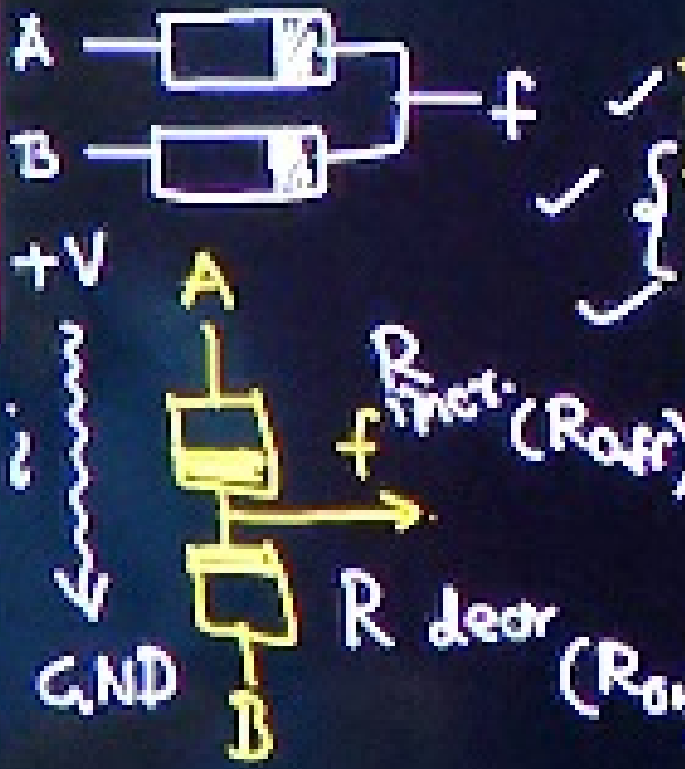
Logic Design:

NAND

$$i = \frac{V}{R_{off} + R_{on}}$$

$$f = i \cdot R_{on} = \frac{R_{on} \cdot V}{R_{off} + R_{on}} \approx$$

(a) Memristor Ratioed Logic (MRL)



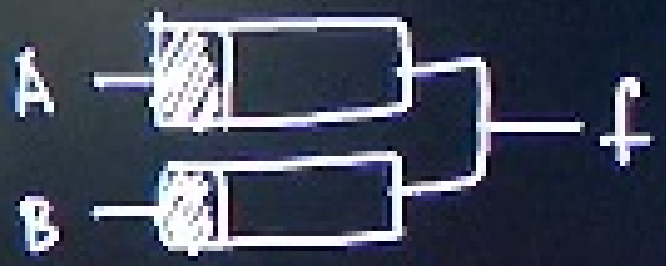
A	B	f
0	0	0
0	1	0
1	0	0
1	1	1

AND

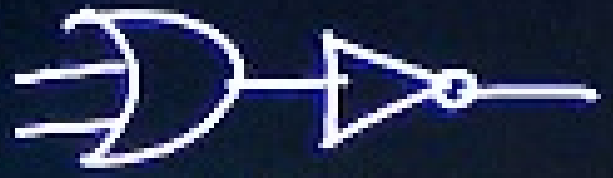
0 ← Low voltage (GND)

1 ← High voltage (V_{DD})

CMOS Inverter



A	B	f
0	0	0
0	1	1
1	0	1
1	1	1



NOR

OR

$$i = \frac{V}{R_{on} + R_{off}}$$

$$f = i \cdot R_{off} = \frac{V \cdot R_{off}}{R_{on} + R_{off}} = \frac{V}{R_{on}/R_{off} + 1}$$

$$\approx V$$